

10/026,466
01USFP707-R.M.

REMARKS

Claims 1-26 are all the claims presently pending in the application. Claims 1-6 and 9-13 stand rejected on prior art grounds. Claims 16-26 are allowed and claims 7-8 and 14-15 would be allowable if rewritten in independent form.

Claims 1-2, 5, 12, 20, and 25 have been amended to clarify the language of the claims.

No new matter is added to the amended claims. The claims are amended to merely clarify the subject matter of the claims and in not to narrow the scope of the claims in order to overcome the prior art or for any statutory purposes of patentability. Notwithstanding any claim amendments of the present Amendment or those amendments that may be made during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Reconsideration in view of the foregoing amendments and the following remarks is respectfully solicited.

Attached hereto is a marked up version of the changes made in the specification and/or claims by the current Amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Claims 1-4, 6, 9-11, and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Geysen (U.S. Patent No. 6,229,376). Claims 5 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Geysen in view of Kipnis (U.S. Patent No. 6,326,836).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention, as disclosed and claimed, for example by independent claim 1,

10/026,466
01USFP707-R.M.

is directed to a driving circuit (and a constant current driving apparatus using the driving circuit). The driving circuit includes a first current mirror circuit and a second current mirror circuit. The first current mirror circuit outputs a plurality of output currents, each of which corresponds to a reference current, and a second current mirror circuit which converts a polarity of an output current outputted from a final stage of the first current mirror circuit and outputs the converted output current, as recited in claim 1.

The conventional driving circuit has a current mirror circuit to drive a load at a constant current. This circuit employs the method of independently setting an input current of the current mirror circuit by adjusting the resistive value. Thus, it is difficult to reduce variation in the reference currents of driving circuits when a plurality of driving circuits are used to drive, such as an LED panel, a device at a constant current. As the position of a transistor is located farther away from the power supply terminal, the deviation in the current ratio is increased. This causes, for example, a difference between the brightness of a light emission device driven by a transistor located close to the power supply terminal and a brightness of a light emission device driven by a transistor located far from the power supply terminal (Application, p. 1, lines 10-25).

The claimed device, on the other hand, includes a driving circuit that has a first current mirror circuit which outputs a plurality of output currents which correspond to a reference current and a reference current input terminal for supplying the reference current to the first current mirror circuit. A second current mirror circuit converts a polarity of an output current outputted from a final stage that is arranged in a position farthest away from said reference current input terminal, as recited in claim 1.

10/026,466
01USFP707-R.M.

III. THE PRIOR ART REJECTION

The Examiner alleges claims 1-4, 6, 9-11, and 13 are anticipated under 35 U.S.C. § 102(e) by Geysen. Applicant submits, however, that there are elements of the claimed invention which are not found in Geysen.

THE GEYSEN REFERENCE

Geysen discloses an analog node from which a computing network may be constructed. The node comprises a current input to a transistor as part of a current mirror formed by a plurality of transistors such that the transistors mirror the current input to source an equivalent current for connection within a network as positive feedforward, and an equivalent current for connection within a network as positive feedback. (Geysen, col. 11, lines 42-55).

Even assuming arguendo that Geysen has a PNP current mirror circuit and an NPN current mirror circuit, and that the polarity of the output current of the PNP current mirror circuit is inverted by the NPN current mirror circuit, any similarity with the claimed invention stops there.

Specifically, Geysen discloses a mirrored equivalent current that is input to the current mirror with an additional group of transistors such that the additional transistors mirror the current input to sink an equivalent current for connection within a network as a negative feedforward, and an equivalent current for connection within a network as negative feedback (Geysen, col. 11, lines 42-55).

However, Applicant submits that the Geysen reference teaches different objectives and

10/026,466
01USFP707-R.M.

matters as the present application. In the present invention, the first current mirror circuit (e.g., a PNP transistor in a nonlimiting exemplary embodiment) has a plurality of outputs, each of which corresponds to a reference current supplied from a terminal, and a second (e.g. NPN) current mirror circuit which converts a polarity of an output current outputted from a final stage of the first mirror circuit, where the final state of the first mirror circuit is arranged in a position farthest away from a reference current input terminal, as recited in claim 1. Thus, using a suitable selection of a reference current and resistance in the first current mirror circuit, all of the driving circuits in the series have substantially the same output current values (Application, p. 20, lines 5-10).

Hence, turning to the clear language of claim 1, there is no disclosure or suggestion of “a final stage of said first current mirror circuit” that “outputs the converted output current, wherein said final stage of said first current mirror circuit is arranged in a position farthest away from said reference current input terminal.” Thus, the output current of the first current mirror circuit of the last stage is outputted through the second current mirror circuit. When a plurality of constant current driving circuits are used, a linear output can be achieved.

On the other hand, the reference merely has the objective of inverting the current polarity by the first and second current mirror circuits. Geysen teaches using complementary mirrors as nodes within a computer network for transmitting information in a feedforward or feedback manner through the network (Geysen, col. 6, lines 23-27). Geysen does not disclose or suggest “a first current mirror circuit which outputs a plurality of output currents each of which corresponds to a reference current” such that the first transistor of a series within the first current mirror circuit is physically arranged at the closest position to a power supply terminal, and “a reference current input terminal supplying a reference current to said first

10/026,466
01USFP707-R.M.

current mirror circuit. . . wherein said final stage of said first current mirror circuit is arranged in a position farthest away from said reference current input terminal.” as recited in claim 1.

For at least the reasons outlined above, Applicant respectfully submits that Geysen fails to teach or suggest every feature of claim 1. Accordingly, Geysen fails to anticipate the subject matter of claim 1 and claims 1-4, 6, 9-11, and 13, which depend from claim 1. Withdrawal of the rejection of claims 1-4, 6, 9-11, and 13 under 35 U.S.C. § 102(e) as being anticipated by Geysen is respectfully solicited.

THE KIPNIS REFERENCE

The Examiner rejected claims 5 and 12 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Geysen in view of Kipnis (U.S. Pat. No. 6,323,836). Applicant submits, however, that there are elements of the claimed invention which are not found in Geysen or Kipnis.

The deficiencies of Geysen have been described above. Kipnis fails to make up the deficiencies.

Specifically, Kipnis discloses a bias circuit with an input current having a first reference node, the input current being gain divided to form a current smaller than the input current by a magnitude of the gain (Kipnis, abstract).

The Examiner alleges that, in reference to Claim 5 of the present application, the Kipnis reference discloses that each of the current mirror circuits in Figure 2 includes a current compensation circuit for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit. The Examiner makes a similar rejection to Claim 12 as Claim 5 where claim 12 is the “reversed Figure 2 of the Geysen reference and that

10/026,466
01USFP707-R.M.

Kipnis discloses at least one of the current mirror circuits in Figure 2 includes a current compensation circuit for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit.

The structure of the Kipnis reference is different from that of the present invention. Unlike the present invention, Kipnis does not have a first (e.g. PNP) current mirror circuit with a plurality of outputs.

Kipnis has a gain converting means for converting input current I_{in} into current I_{in}/hfe once. Finally, the output current I_{out} is $I_{in}/hfe^2 \cdot hfe = I_{in}$. when hfe of the gain converting means is not equal to the of the output stage, the output current with the same value as that of the input current cannot be obtained. Additionally, in the present invention, it is possible to transfer a reference current to the output of the second (e.g. NPN) current mirror circuit correctly by using the first and second current mirror circuits.

Certainly no person of ordinary skill in the art would consider combining such references, absent hindsight. Indeed, the Examiner has not cited a prior art reference that suggests in some way a modification of a particular reference or a combination with another reference in order to arrive at the claimed invention. The prior art items themselves must suggest the desirability and thus the obviousness of making the combination independent of the present invention. ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577; 221 USPQ 929, 933 (Fed. Cir. 1984); In re Geiger, 815 F.2d 686, 688; 2 USPQ2d 12276, 1278 (Fed. Cir. 1987) (Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination).

Therefore, contrary to the allegations of the Examiner, the combination of Geysen and

10/026,466
01USFP707-R.M.

Kipnis cannot teach or suggest the claimed invention, as a whole, of “a first current mirror circuit which outputs a plurality of output currents each of which corresponds to a reference current, a reference current input terminal supplying a reference current to said first current mirror circuit, and a second current mirror circuit which converts a polarity of an output current outputted from a final stage of said first current mirror circuit and outputs the converted output current, wherein said final stage of said first current mirror circuit is arranged in a position farthest away from said reference current input terminal,” as recited in claim 1. Kipnis clearly fails to make up for Geysen’s deficiencies.

Therefore, Applicant respectfully submits that these references would not have been combined as alleged by the Examiner and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Geysen and Kipnis fail to render obvious claims 5 and 12, which depend from claim 1. Withdrawal of the rejection of claims 5 and 12 under 35 U.S.C. § 103(a) as unpatentable over Geysen in view of Kipnis is respectfully solicited.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

IV. INFORMAL MATTERS AND CONCLUSION

Claims 5, 12, 20, and 25 have been corrected to overcome the Examiner’s objections. Specifically, the statement “said first” has been changed to --said first current mirror-- in each of the referenced claims.

The drawings have been corrected to show elements of claims 7-8 and 14-15, as specified by the Examiner. No new matter was added to the drawings.

10/026,466
01USFP707-R.M.

In view of the foregoing, Applicant submits that claims 1-26, all the claims presently either rejected or objected to in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to withdraw the rejections and pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner may contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: Jan. 7, 2003



Kendal M. Sheets
Reg. No. 47,077

Sean M. McGinn
Reg. No. 34,386

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254

VERSION WITH MARKINGS TO SHOW CHANGES MADE**IN THE SPECIFICATION:****Please amend paragraph 1, on page 21:**

Fig. 7 is a circuit diagram showing the configuration of the driving circuit according to the second embodiment. In this driving circuit, a first current mirror circuit 10a is configured such that a PNP transistor Tr_x serving as the base current compensating circuit 21 is added to the first current mirror circuit 10 of the driving circuit according to the first embodiment.

Please amend paragraph 2, on page 21:

A base of the PNP transistor Tr_x 21 is connected to the collector of the PNP transistor Tr_o , an emitter is connected to the base of the PNP transistor Tr_o , and a collector is connected to a ground terminal 14.

Please amend paragraph 4, on page 21:

Also, a second current mirror circuit 20a is configured such that an NPN transistor Tr_y serving as a base current compensating circuit 22 is added to the second current mirror circuit 20 of the driving circuit according to the first embodiment.

Please amend paragraph 1, on page 22:

A base of the NPN transistor Tr_y 22 is connected to the collector of an NPN transistor Tr_a , an emitter is connected to the base of the NPN transistor Tr_a , and a collector is connected to a second power supply terminal 15. A power supply suitable for compensating the base current of the NPN transistor Tr_a is impressed to the second power supply terminal 15.

Please amend paragraph 2, on page 22:

The addition of the base current compensating circuit constituted by the NPN transistor Tr_y 22 enables a collector current I_c of the NPN transistor Tr_a to be closer to the reference current I_{ref} even if the base current can not be ignored.

10/026,466
01USFP707-R.M.

Please amend paragraph 4, on page 22:

It should be noted that the second embodiment is designed such that the base current compensating circuit is installed in each of the first current mirror circuit 10a and the second current mirror circuit 20a. However, as shown in Fig. 8, the base current compensating circuit 22 may be installed only in the second current mirror circuit 20a. Also, as shown in Fig. 9, the base current compensating circuit 21 may be installed only in the first current mirror circuit 10a.

Please amend paragraph 1, on page 35:

Fig. 16 is a circuit diagram showing a configuration of the driving circuit according to the seventh embodiment of the present invention. This driving circuit is equal to that of the first embodiment except that the power supply terminal 11 is disposed at a physical center 23 of a common power supply line 16 through which emitters of NPN transistors Tr_o to Tr_{n+1} are connected to each other. Here, the center 23 implies a portion between a first portion where the emitter of the PNP transistors Tr_o is formed and a second portion where the emitter of the PNP transistor Tr_{n+1} is formed. Preferably, the center 23 may be located at a substantial center between the first portion and the second portion.

Please amend paragraph 2, on page 35:

According to this configuration, an output current outputted from the output terminal at the center 23 out of output currents outputted from the output terminals O_1 to O_n of the driving circuit is the largest. The output currents become gradually smaller toward the side of the output terminal O_1 and the side of the output terminal O_n . That is, they form a shape of a mountain.

Please amend paragraph 2, on page 36:

It should be noted that the driving circuit according to the fifth embodiment can be also configured so as to pull out the power supply terminal 11 from the center 23 of the common power supply line 16. Also, the third and fourth embodiments can be configured so as to pull out the ground terminal 14 from the center 25 of the common ground line 17. All of

10/026,466
01USFP707-R.M.

the cases can provide the effects similar to the above-mentioned effects.

Please amend paragraph 1, on page 37:

Fig. 17 is a circuit diagram showing a configuration of a variation of the driving circuit according to the seventh embodiment of the present invention. This driving circuit is equal to that of the first embodiment except that the power supply terminal 11 is pulled out from a plurality of positions 24 of the common power supply line 16 through which the PNP transistors Tr_o to Tr_{n+1} are connected. This case can be configured such that the common power supply line 16 is divided into m components (" m " is an integer equal to or greater than 3) and $(m-1)$ wires are pulled out from the respective divided points 24 and connected to the power supply terminal 11. Fig. 17 shows an example of a case of " $m=3$ ". It should be noted that when the common power supply line 16 is divided into the m components, it is desired to be divided such that a length of a division piece at each of both ends among the m division pieces becomes half that of the division piece except both ends. For example, in the example of " $m=3$ " shown in Fig. 17, the common power supply line 16 is desired to be divided at a rate of 1:2:1. However, it is not always necessary to divide the common power supply line 16 as mentioned above.

Please amend paragraph 1, on page 39:

It should be noted that the driving circuit according to the fifth embodiment can be also configured so as to pull out the power supply terminal 11 from the plurality of positions 24 of the common power supply line 16. Also, the third and fourth embodiments can be configured so as to pull out the ground terminal 14 from the plurality of positions 26 of the common ground line 17. All of these cases can provide the effects similar to the above-mentioned effects provided by the variation of the seventh embodiment.

IN THE CLAIMS:

Claims 1-2, 5, 12, 20, and 25 have been amended, as follows:

1. (Amended) A driving circuit comprising:
a first current mirror circuit which outputs a plurality of output currents each of which


10/026,466
01USFP707-R.M.

corresponds to a reference current; [and]

a reference current input terminal for supplying said reference current to said first current mirror circuit; and

a second current mirror circuit which converts a polarity of an output current outputted from a final stage of said first current mirror circuit and outputs the converted output current[.].

wherein said final stage of said first current mirror circuit is arranged in a position farthest away from said reference current input terminal.



2. (Amended) The driving circuit according to claim 1, wherein said first current mirror circuit [comprising] comprises:

[a reference current input terminal to which said reference current is supplied;]

a power supply terminal to which power is supplied;

a first circuit provided between said reference current input terminal and said power supply terminal, to determine said plurality of output currents;

a common power supply line which extends from said power supply terminal;

a plurality of output terminals;

a plurality of second circuits provided between said common power supply line and said plurality of output terminals, to output a part of said plurality of output currents determined by said first circuit through said plurality of output terminals; and

a third circuit provided at a next stage of said plurality of second circuits as said final stage of said first current mirror circuit, to output said output current determined by said first circuit.

5. (Amended) The driving circuit according to claim 4, wherein at least one of said first current mirror circuit and said second current mirror circuit [has] includes a base current compensating circuit.

12. (Amended) The driving circuit according to claim 11, wherein at least one of said first current mirror circuit and said second current mirror circuit [has] includes a base current

10/026,466
01USFP707-R.M.

compensating circuit.

20. (Amended) The constant current driving apparatus according to claim 19, wherein at least one of said first current mirror circuit and said second current mirror circuit [has] includes a base current compensating circuit.

25. (Amended) The constant current driving apparatus according to claim 24, wherein at least one of said first current mirror circuit and said second current mirror circuit [has] includes a base current compensating circuit.